WHAT IS CLAIMED IS:

1. A nonvolatile memory comprising:

a first terminal;

a second terminal;

a controller; and

nonvolatile memory cells,

wherein said first terminal is for receiving pulses of a first signal,

wherein said second terminal is for receiving data, and

wherein said controller is adapted to control (i) the receiving of address information, (ii) the receiving of data via said second terminal in response to the pulses of said first signal received from said first terminal, and (iii) the performing of data writing to ones of said nonvolatile memory cells corresponding to said address information without receiving pulses of said first signal via said first terminal.

2. A nonvolatile memory according to claim 1,

wherein said nonvolatile memory controls the performing of a verify operation for checking whether said data writing is completed or not, after performing said data writing without receiving pulses of said first signal via said first terminal.

3. A nonvolatile memory according to claim 2, further comprising a power generating circuit,

wherein said power generating circuit is configured to generate a program voltage for use in writing said data, and

wherein said controller enables said power generating circuit to generate said program voltage during said data writing.

4. A nonvolatile memory according to claim 3,

wherein said controller is capable of receiving a 512 Byte length unit as said data, and

wherein said ones of nonvolatile memory cells corresponding to said address information are capable of storing data of more than 512 Bytes in length.

5. A nonvolatile memory comprising:

a first terminal;

a second terminal;

a controller; and

a plurality of nonvolatile memory arrays,

wherein said first terminal is capable of receiving pulses of a first signal,

wherein said second terminal is capable of receiving data,

wherein each of said plurality of nonvolatile memory arrays includes a plurality of nonvolatile memory cells,

wherein said controller is adapted to control (i) the receiving of a first address information, (ii) the receiving of first data via said second terminal in response to the pulses of said first signal, and (iii) the selecting of a first one of said plurality of nonvolatile memory arrays, corresponding to said first address information, and the writing of said first data therein, and

wherein said first one of said plurality of nonvolatile memory arrays is capable of performing writing of said first data to ones of said plurality of nonvolatile memory cells therein corresponding to said first address information without receiving pulses of said first signal.

6. A nonvolatile memory according to claim 5,

wherein said controller further controls (iv) the receiving of a second address information, (v) the receiving of a second data via said second terminal in response to the pulses of said first signal, and (iv) the selecting of a second one of said plurality of nonvolatile memory arrays, corresponding to said second address information, and the writing of said second data therein, and

wherein said second one of said plurality of nonvolatile memory arrays is capable of performing writing of said second data to ones of said nonvolatile memory cells therein corresponding to said second address information without receiving pulses of said first signal.

7. A nonvolatile memory according to claim 6,

wherein each of said plurality of nonvolatile memory arrays performs a verify operation for checking whether or not data writing is completed therein, in the performance of a writing operation.

8. A nonvolatile memory according to claim 7,

wherein each of said plurality of nonvolatile memory arrays performs an erase operation for erasing data stored in ones of said plurality of nonvolatile memory cells, and

wherein said second one of said plurality of nonvolatile memory arrays is capable of performing said erase operation for erasing data stored in ones of nonvolatile memory cells therein corresponding to said second address information in a writing operation of said first data in said first one of said plurality of nonvolatile memory arrays.

9. A nonvolatile memory according to claim 8,

wherein each of said first data and said second data is 512 Bytes in length, and

wherein said ones of said nonvolatile memory cells in said first one of nonvolatile memory arrays are capable of being written with more than a 512 Byte length data, and

wherein said ones of said nonvolatile memory cells in said second one of nonvolatile memory arrays are capable of being written more than a 512 Byte length data.